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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,555	03/22/2001	David B. Squires	X-857 US	6451

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
HUYNH, KIM NGOC	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,555	SQUIRES, DAVID B.	
	Examiner	Art Unit	
	Kim Huynh	2182	

-- Th MAILING DATE of this communication appears on th cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 10-13* is/are pending in the application.

4a) Of the above claim(s) *15-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 15-22 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the configurable I/O block and the lookup table of the configurable logic device are of different scope than the originally presented claimed invention.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 14-22 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Specification

2. The incorporation of essential material in the specification by reference to a foreign application or patent, or to a publication is improper. In this instant, the limitation *programmable routing matrix* is essential to the claim and is not found in the specification.

Applicant is required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or a practitioner representing the applicant, stating that the

amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

"Essential material" is defined as that which is necessary to (1) describe the claimed invention, (2) provide an enabling disclosure of the claimed invention, or (3) describe the best mode (35 U.S.C. 112). In any application which is to issue as a U.S. patent, essential material may not be incorporated by reference to (1) patents or applications published by foreign countries or a regional patent office, (2) non-patent publications, (3) a U.S. patent or application which itself incorporates "essential material" by reference, or (4) a foreign application.

Mere reference to another application, patent, or publication is not an incorporation of anything therein into the application containing such reference for the purpose of the disclosure required by 35 U.S.C. 112, first paragraph. In re de Seversky, 474 F.2d 671, 177 USPQ 144 (CCPA 1973). See MPEP § 608.01(p).

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "programmable routing matrix... logic block" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 4-6, 10, are rejected under 35 U.S.C. 102(b) as being anticipated by Akao (US 5,307,464).

a. Claims 1, 6, Akao discloses (Figs. 1-2 and 8-10) a system having menu allowing user to select one of a plurality of configurable logic devices (see Fig. 10), an integrated circuit 1 (see Figs. 1-2) having a bus 7 connecting a processor core 2 to a configurable peripheral device 5 having a configurable logic block (functional logic loaded from the ROM to RAM and subprocessor 5) (see col. 6, l. 25 to col. 7, l. 8) capable of implementing a plurality of logic functions (col. 2, ll. 10-17, 47-67 and col. 3, l. 59 through col. 4, l. 9); and a programmable routing matrix coupling to the logic block for routing the signals to and from the CLB (RAM array address control circuit for selecting column and row addresses, see at least Fig. 6 and 15).

b. Claims 2, 5, and 10, Akao discloses the configurable peripheral devices (peripheral functions) are versatile and can be of counter, timer, serial communication (UART), ROM, RAM (flash memory controller) (col. 1, l. 30-47).

c. Claim 4, Akao discloses the peripheral and bus are implemented on a FPGA (see Figs. 15-17 and 20). Please note memory arrays of Akao are field programmable and therefore meet the definition of FPGA.

Akao does not disclose the specific structure of the programmable logic control as claimed. However, Akao suggested that his invention can be implemented using PLD or PLA (col. 32, ll. 27-32).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6, 10-13 are rejected under 35 U.S.C. 103(a) as being obvious over "The Programmable logic data Book 2000" in view of Akao (US 5,307,464).

a. Claims 1, 4, 6, "The Programmable logic data Book 2000" discloses a Virtex-E FPGA device having all the feature of a CLB as claimed (programmable routing matrix, configurable I/O block and lookup table, see p. 3-7 to 3-12) for providing a high speed and high capacity programmable logic solution to enhance design flexibility (the Virtex_E FPGA is described in a printed publication and in public use/sale in this country, more than one year prior to the date of the instant application). It is inherent that the Virtex_E FPGA when in use would coupled to a core processor via a bus in order to perform its function.

As for the limitation of using the FPGA to implementing the functions of peripheral devices, Akao discloses that it is well known in the art to implement a single chip microprocessor having embedded configurable hardware logic with a processor (CPU 2) to provide various peripheral functions (col. 1, ll. 29-65) It would have been obvious to one having ordinary skill in the art to utilize the Vertex_E FPGA in providing the peripheral functions in order to take advantage of a commercially available product which offers a high speed and high capacity programmable logic solution to enhance design flexibility of the peripheral device and allow the peripheral functions to be defined more easily and as defined by the user (Akao, col. 1, ll. 50-65).

Furthermore, please note recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

b. Claims 2, 5, and 10, Akao discloses the configurable peripheral devices (peripheral functions) are versatile and can be of counter, timer, serial communication (UART), ROM, RAM (flash memory controller) (col. 1, l. 30-47).

8. Claims 3, 11-13 are rejected under 35 U.S.C. 103(a) as being obvious over Akao (per 35 USC 102 above) or "The Programmable logic data Book 2000" in view of Akao (per 35 USC 103 above) and further in view of applicant's admission (paragraphs 15-16).

As for the specific user selectable options (baud rate, width size, and error correction selector); please note baud rate, width size, and error correction codes are property of a particular peripheral device to enhance its transmission operation. Since the combination of Akao and the Vertex_E FPGA above discloses a flexible and versatile system allowing the users to easily set and modify the peripheral functions in the his own way via programmable logic control (background and summary of the invention). Applicant admitted that the choice of user selectable options are various and can be tailored to meet the needs of the user; therefore, it would have been obvious to one having ordinary skill in the art to modify the system of Akao for the user to select

options that is related to the peripheral being connected to the system based on the user's need and the operational specification of the peripheral device as intended Akao (col. 1, ll. 7-17).

Response to Arguments

9. Applicant's arguments filed 10/22/04 have been considered but are moot in view of the new ground(s) of rejection necessitated by the amendment. The examiner also maintains the rejection of Akao and respond to the applicant's argument are as followed:

Applicant seem argues the RAM/EEPROM of Akao are not configurable logic block. Please note these memory arrays are field programmable and therefore meet the definition of configurable logic block. It is unclear what applicant's definition of "configurable logic block" is if they are different from the known memory arrays that are programmable. The examiner also submits the Southgate (US 5,968,161) reference which discloses that programmable/configurable logic device are implemented using various type of programmable devices such as FPGA, SPGA, EPROM, PAL, and PLA (col. 4, ll. 23-29) to further support her position.

Applicant further argues that Akao teaches away from employing configurable logic in a microprocessor based IC citing Akao uses software to perform the selected peripheral functions instead of hardwired logic configuration. Please note Akao uses software to control the logic of the RAM by loading/configuring the appropriate peripheral function as selected by the user into the memory of the sub-processor 5.

This is how programmable devices are configured, it is in the same manner as the Virtex-E FPGA since the Virtex-E FPGA is a SRAM based customized to load configuration data read from external ROM (page 3-6, right column, second paragraph).

Does the applicant imply that his "configurable logic control" does not function in this manner? Please note, hardwired logic configuration is not changeable once it is program. Does the applicant imply that his configurable logic control is hardwired? It is not how the examiner interprets the term "configurable logic" or if it is a common definition in the art.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Southgate (US 5,968,161) discloses that programmable/configurable logic device are implemented using various type of programmable devices such as FPGA, SPGA, EPROM, PAL, and PLA (col. 4, ll. 23-29).

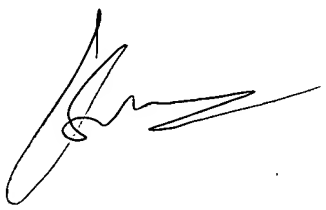
11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571) 272-4147.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.



Kim Huynh
Primary Examiner
Art Unit 2182

KH
12/14/04.